Gap states in silicon nitride

John Robertson and Martin J. Powell

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might be attributed to the decrease of the gap state density due to the increase of the Si-H content.

In summary, we have shown that there is a correlation between V_b and the desirable properties. It might be attributed to the enhanced incident ion flow due to rf voltage application.

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Gap states in silicon nitride

John Robertson
Central Electricity Research Laboratories, Leatherhead, Surrey, United Kingdom

Martin J. Powell
Philips Research Laboratories, Redhill, Surrey, United Kingdom

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The energy levels of defect states in amorphous silicon nitride have been calculated and the results are used to identify the nature of trap states responsible for charge trapping during transport and the charge storage leading to memory action. We argue that the Si dangling bond is the memory trap in chemical vapor deposited memory devices and is also the center in plasma-deposited nitride responsible for hopping at low electric fields and for charge-trapping instabilities in amorphous silicon-silicon nitride thin-film transistors.

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Silicon nitride forms the memory medium in nonvolatile metal-nitride-oxide-semiconductor (MNOS) devices[1,2] and is used as a dielectric in thin-film transistors.[3–5] Although these applications of silicon nitride depend crucially on the behavior of its gap states, our understanding of them is incomplete.[2] In this letter we develop a schematic gap state energy distribution based on the calculated energy levels of the principal defects, namely, the Si and N dangling bonds (≡Si and =N), ≡SiH and =NH units, and the ≡Si-Si≡ unit, and then use the distribution to interpret conduction and charge storage processes.

The concentration of the various defects depends on the deposition process involved: chemical vapor deposition (CVD) or plasma deposition (PD). Although the resulting stoichiometry can be varied in both CVD[6] and PD[7] films, the common situation is that PD films tend to be Si rich whereas CVD films are much closer to stoichiometric Si_3N_4. Both CVD and PD films also contain chemically bonded hydrogen, from up to 30% H in the lower temperature PD process, to perhaps 4–10% in CVD films[8] with very few ≡SiH units in CVD films prepared above 900 °C. Hydrogen combines with dangling bonds and removes their gap states in amorphous silicon (*a*-Si). By analogy with PD and CVD *a*-Si:H, we expect similar passivation in silicon nitride and also a much lower dangling bond concentration in PD nitride. Thus, PD nitride will contain up to 30% of ≡SiH and =NH units, 1%–10% of ≡Si-Si≡ units and 10^{17} cm^{-3} dangling bonds while CVD nitride contains, say, 5% of ≡SiH units, less than 1% of ≡Si-Si≡ units and about 10^{19} cm^{-3} dangling bonds. Furthermore, since the constraints of the random network causing bonds to break increase with coordination number,[9] Si dangling bonds will outnumber =N centers.

The local electronic structure of the principal defects was calculated by the tight-binding recursion method,[10] and the results are indicated in Fig. 1. The =NH center does not produce gap states. The neutral $=N^0$ center has an enhanced peak at the valence-band maximum. The charge of

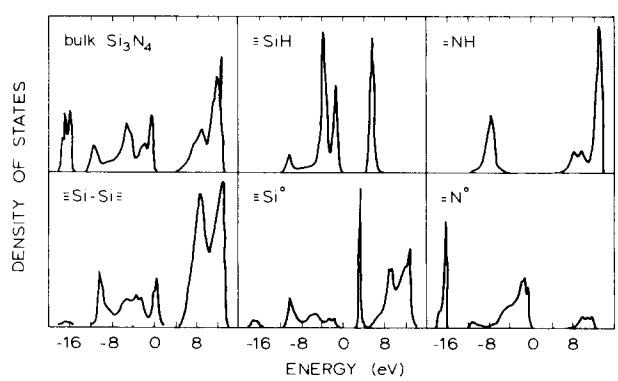

FIG. 1. Local density of states for (a) bulk Si_3N_4, (b) H site at ≡SiH centers, (c) H site at =NH centers, (d) Si–Si centers, (e) ≡Si centers, and (f) =N centers. The zero of energy is the valence-band maximum of the bulk.

$\equiv N^-$ binds a state above the valence edge, like in the negative nonbridging oxygen of SiO_2.[11] Also as in SiO_2,[11] we must introduce self-energy shifts at the Si centers. Si uses its four sp^3 hybrids for bonding in both Si_3N_4 and Si, but a Si hybrid must be assigned a higher energy in a Si–N bond, to give the observed 1.9-eV conduction-band discontinuity at $Si:Si_3N_4$ interfaces.[12] This same shift is then used for the specific Si hybrids in Si–Si and Si–H bonds and Si dangling bonds in Si_3N_4.[13] The $\equiv Si^0$ centers give gap states at 3.1 eV, 80% localized on site. The bonding (σ) state of Si–Si centers is found to lie just in the gap, at about 0.1 eV, and the antibonding state (σ^*) is in the conduction band. Both σ and σ^* Si–H states lie just outside the gap, as in a-Si:H, so H acts as a passivant.

We can now construct gap state spectra for CVD and PD nitrides, taking into account their different compositions and defect concentrations (Fig. 1). The $\equiv Si$ centers produce a density of states peak near midgap. As $\equiv Si$ centers outnumber $\equiv N$ centers, the latter are doubly occupied and negatively charged and the Fermi level lies within the $\equiv Si$ states. Consequently, at equilibrium some $\equiv Si$ centers are paramagnetic and neutral while some are positively charged. The full occupation of $\equiv N^-$ centers accounts for the detection of only Si dangling bonds by electron spin resonance, and an earlier suggestion of preferential hydrogen passivation of $\equiv N$ centers is not now needed.[14] The Si–Si centers and $\equiv N^-$ centers generate a valence-band tail of about 1.5-eV width. Gap states attributed to Si–Si bonds and Si dangling bonds have been observed close to these calculated positions in radiation damaged Si_3N_4.[15]

CVD silicon nitride exhibits Poole–Frenkel hole conduction.[16,17] We identify the $\equiv N^-$ centers as the hole traps involved, being charged when empty. In PD nitride, the neutral Si–Si centers are expected to dominate hole conduction, if we take the cross section of neutral traps to be 10^{-4} times that of charged traps. We can now also account for why electrons and holes dominate conduction in SiO_2 and Si_3N_4, respectively. SiO_2 is much purer and more defect free than Si_3N_4 so conduction is less dependent on defects. The electron effective mass of SiO_2 is quite low, while holes form self-trapped polarons, so electrons dominate. In Si_3N_4, holes hop through to relatively shallow traps of its valence tail while electrons become trapped by the very deep $\equiv Si^+$ centers. The $\equiv Si$ centers also act as traps in SiO_2, but their density is much lower, say 10^{14} cm^{-3} (Ref. 11) compared to 10^{19} cm^{-3} in CVD nitride.

We propose that $\equiv Si$ centers are the long term (memory) traps of CVD nitide in MNOS devices. However, unlike in the models of Kirk[18] and Ngai and Hsia,[19,20] we argue that dangling bonds have a positive not negative correlation energy. The $\equiv Si$ center acts as a memory trap because it is amphoteric, deep, and energetically aligned with the gap of Si. Thus, $\equiv Si$ centers trap either electrons or holes during the write process and release them during reading. The shift of the write/read window after repetitive cycling is now generally associated with defect creation at the $Si:SiO_2$ interface.[21]

Both the $\equiv Si$ and $\equiv N$ centers have positive correlation energies (U). The concept of negative U was introduced to describe electron transitions at defects strongly coupled to the lattice, such as the valence alternation pairs of amorphous chalcogenides. Two processes can produce a negative U: valence alternation and overcoordination (as in a-Se) or rehybridization due to bond angle changes [as in the 2×1 buckling reconstruction of Si(111) surfaces]. We argued previously,[10,22] that neither $\equiv N^+$ or $\equiv Si^+$ centers could overcoordinate because of the small radius of the second N site involved. Also, $U\simeq0.4$ eV for $\equiv Si$ centers in a-Si:H,[23] and the 2×1 buckling reconstruction is now known to be unstable,[24] so the second mechanism does not apply to Si centers. Additionally the low screening of Si_3N_4 will increase direct electron repulsion and further increase U. Thus, $U>0$ for both $\equiv Si$ and $\equiv N$ centers. The $\equiv Si$ center will thus show two levels, a lower $+/0$ ($\equiv Si^0$) trapped hole level and, U higher, the $0/-$ ($\equiv Si^-$) trapped electron level, as shown in Fig. 2 and as found for the P_b ($\equiv Si$) centers at $Si:SiO_2$ interfaces.[25]

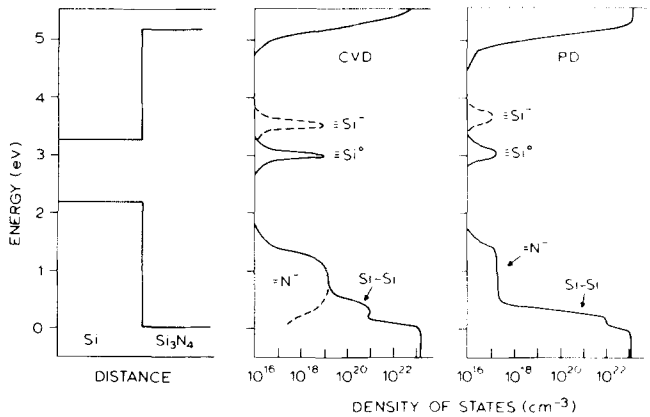

FIG. 2. Proposed densities of gap states for (a) CVD and (b) PD silicon nitride.

From Fig. 2 it is clear that the $\equiv Si$ center is responsible for the hopping conduction observed in silicon nitride at low electric fields,[5] and is thus the principal cause of charge trapping instabilities in amorphous silicon-silicon nitride thin-film transistors.[5] It is interesting to note that the performance of amorphous silicon-silicon nitride thin-film transistors is critically dependent on the density of silicon dangling bonds, situated in both the amorphous silicon layer and the silicon nitride layer. The $\equiv Si$ states in the a-Si layer are in thermal equilibrium with the conduction band on a short time scale, and thus these states control the quasi dc device characteristics in the prethreshold region.[26] On a longer time scale $\equiv Si$ states is the nitride layer trap charge, transferred from the amorphous silicon, which shows itself as a threshold voltage shift in the quasi dc characteristics.[5,26]

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Determination of SiO_2 trapped charge distribution by capacitance-voltage analysis of undoped polycrystalline silicon-oxide-silicon capacitors

Y. Nissan-Cohen, J. Shappir, and D. Frohman-Bentchkowsky
Applied Physics Division, School of Applied Science and Technology, The Hebrew University of Jerusalem, Jerusalem, Israel

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Capacitance measurements on undoped polycrystalline silicon gate capacitors are used for oxide trapping characterization. In this structure, a field-effect modulation on both interfaces is observed in a single C-V plot. A variation in the insulator charge state is detected by its effect on both interfaces. The main advantage of this method is that both trapped charge magnitude and centroid are obtained by a single measurement with a minimal disturbance of the charge distribution. The method is demonstrated on thin oxide capacitors subjected to negative or positive charge trapping. The induced positive and negative charge magnitude and location dependence on the injection conditions are measured and analyzed.

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Charge trapping in SiO_2 has received much attention because of its relation to device degradation and reliability. Many of the studies, which are based on measurement of the flatband voltage of metal-oxide-silicon (MOS) capacitors, or the threshold voltage of MOS devices, do not clarify the complete trapping picture. The information gained by these measurements is not sufficient to separate between bulk and interface charges, or to find both charge magnitude and centroid. Theoretically, two measurement techniques, the photo current-voltage and the tunneling current-voltage analysis, can be used for this purpose.[1–3] However, there are a few restrictions and disadvantages of these two methods. Firstly, the measurements conditions affect the trapped charge distribution either by capture of injected carriers or by charge detrapping. Furthermore, the photocurrent method needs a light transparent electrode. Therefore, it is limited to thin metal (generally Al or Au) gates, and cannot be applied to the commonly used Si gate structure. The significance of this limitation must be reconsidered in light of several studies which show oxide quality and trapping behavior dependence on the gate electrode material.[4]

In this letter we use a measurement technique which overcomes these two major restrictions. Capacitance-voltage (C-V) measurements are performed on large undoped polycrystalline silicon (poly-Si) gate MOS devices, which have been fabricated in a conventional Si gate MOS process with the omittion of the poly-Si doping step. The C-V curves reflect the field-effect modulation of both substrate and gate interfaces. We will show that a single C-V measurement provides the necessary information for the calculation of both trapped charge magnitude and centroid, and apply the method to demonstrate and analyze positive and negative charge trapping phenomena in the oxide.

Measurements were performed on $60\times180\,\mu^2$ MOS devices which have been fabricated in a modified silicon gate MOS process. Oxides of different thicknesses were thermally grown at 920 and 1000 °C, 3% HCl, on p-type doped ($Na = 5\times10^{16}$ cm^{-3} or 5×10^{14} cm^{-3}) ⟨100⟩ wafers. The poly-Si gate was chemical vapor deposited at 775 °C. The source and drain were formed by phosphorus implantation with a dose of 10^{15} cm^{-2} at an energy of 50 keV and subsequent drive-in at a temprature of 1000 °C. The poly-Si gate was masked against the implant by 2000 Å of thermally grown oxide. Following contacts definition and Al deposition, the wafers were annealed for 25 min in a forming gas at 460 °C. To reduce serial resistance, a large aluminum to poly-Si contact was formed over most of the gate area. A cross section of the device is presented in Fig. 1(a).

According to investigations of poly-Si characteristics,[5,6] the undoped poly-Si is expected to have a p-type behavior. Therefore, we consider a poly-Si oxide-Si (pSOS) structure with a p-doped Si substrate and p-doped poly-Si

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